Please enter the following new paragraph at page 17, after line 30 of the specification as follows:

--Furthermore, in Figure 3, reference numeral 300 denotes a wiring pattern formed on the electric insulating layer 305, and 301 denotes a bare semiconductor chip that is an active component mounted on the wiring pattern 300. Furthermore, reference numeral 302 denotes an electric insulating layer formed of a composite material composed of an inorganic filler and a thermosetting resin. Furthermore, reference numeral 303 denotes an inner via for electrical connection between the wiring patterns 300 formed on the core layer 304.--

B2

Please enter the following new paragraph at page 18, after line 4 of the specification as follows:

--Furthermore, reference number 400 denotes a wiring pattern, and 401 denotes a bare semiconductor chip that is an active component mounted on the wiring pattern 400. Furthermore, reference numeral 402 denotes an electric insulating layer formed of a composite material composed of an inorganic filler and a thermosetting resin. Reference numeral 403 denotes an inner via for electrical connection between the wiring patterns 400 formed on the electric insulating layer 402.--

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Please enter the following new paragraph at page 18, after line 18 of the specification as follows:

--Furthermore, reference numeral 504 denotes a wiring pattern, and 502 denotes an electric insulating layer formed of a composite material composed of an inorganic filler and a thermosetting resin. Reference numeral 503 denotes an inner via formed on the core layer 505.--

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Please replace the paragraph beginning at page 19, line 34 of the specification with the following new paragraph:

-- Next, Figure 6D shows a state in which the product that was superimposed is heated and pressed by a press, so that the semiconductor 601 and the chip component 604

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are buried to be integrated into the sheet material 602. At this time, the components are buried in a state before the thermosetting resin in the sheet material 602 is cured, and further heating is carried out to be cured and thus the thermosetting resin in the sheet 602 and the thermosetting resin in the conductive resin are cured completely. This process allows the sheet material 602, the semiconductor 601, the chip component 604 and the copper foil 600 be adhered strongly to each other mechanically. Similarly, the conductive paste is cured for an electrical connection between the copper foils 600. Next, as shown in Figure 6E, the copper foil on the surface of the substrate in which the thermosetting resin is cured and the semiconductor 601 is buried and integrated is processed into a wiring pattern 600. Thus, a core layer 605 is formed. Figure 6F shows a state in which the core layer 605 is sandwiched between sheet materials 606 formed of a mixture including an inorganic filler and an uncured state thermosetting resin or organic films having adhesive layers on both surfaces, on which a through hole is formed and the through hole is filled with a conductive paste; and then the copper foils 608 are further superimposed thereon. Then, heating and pressing are carried out, thereby forming a wiring layer on both surfaces of the core layer 605 as shown in Figure 6G. Then, as shown in Figure 6H, the adhered copper foils 608 are subjected to a chemical etching so as to form a wiring pattern 609. Thus, a component built-in module can be obtained. Thereafter, steps for mounting components by soldering or filling of an insulating resin are carried out, but such steps are not essential herein, so the explanation therefore is omitted herein. Note here that in Figures 6F to 6H, reference number 607 denotes an inner via.

B5 cont.

Please replace the paragraph beginning at page 21, line 28 with the following new paragraph:

-- Next, in Figure 7G, the component built-in core layer 706 produced by the above-mentioned process is sandwiched between the sheet material 707 produced according to the method described with reference to Figure 7D and the release carrier 710 on which a film-shaped component 711 is formed in a suitable position, followed by heating and pressing. Thus, the multilayer module can be produced as shown in Figure 7H. Finally, as shown in Figure 7I, by peeling off the release carrier 710, the multilayer

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module of the present invention can be produced. Thus, by using the core layer in which the semiconductor and the chip component are contained and the release carrier on which the wiring pattern and film-shaped components are formed, it is possible to obtain a component built-in module having higher density and various functions. Note here that in Figures 7G to 7I, reference numeral 708 denotes an inner via, and 709 denotes a wiring pattern.

B6 Cont.

Please replace the paragraph beginning at page 22, line 3 with the following new paragraph:

--Figures 8A to 8D show cross-sectional views showing a process for producing a component built-in module obtained by laminating onto a multilayer ceramic substrate. Figure 8A shows a core layer 805 in which components are contained, which is shown in Figure 6E. Note here that reference numeral 801 denotes a wiring pattern, 803 denotes an electric insulating layer and 804 denotes an inner via. Then, Figure 8B shows a state in which the core layer 805 and a multilayer ceramic substrate 809 are used and a sheet material provided with an inner via 811 and a sheet material similarly provided with the inner via 813 are superimposed as shown in Figure 8B and then a copper foil 814 is further superimposed. Next, as shown in Figure 8C, by heating and pressing the laminate the thermosetting resins in the sheet materials 810 and 812 are cured, so that the core layer 805 and the multilayer ceramic substrate 809 and copper foil 814 are strongly adhered to each other mechanically. As shown in Figure 8D, by finally processing the copper foil 814 into a wiring pattern and by providing a solder ball 815, a component built-in module in which the multilayer ceramic and the component built-in core layer are integrated is completed. Furthermore, the multilayer ceramic wiring substrate is formed by using a green sheet formed of low temperature firing material mainly including glass and alumina. Namely, the green sheet capable of firing at about 900°C is provided with a through hole and the through hole is filled with a conductive paste including a highly conductive powder such as copper and silver, and furthermore, the wiring pattern is formed by printing a similar conductive paste. A plurality of the green sheets formed by the above-mentioned process are laminated and further fired so as to form the low temperature firing material. The ceramic substrate material produced by the above-

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mentioned process may use a high dielectric material mainly including barium titanate, a high thermal conductive material mainly including aluminum titanate, etc., or the like. Furthermore, the wiring pattern of the outermost layer of the ceramic laminate may be formed or only ceramic laminate may be formed without forming the wiring pattern. Furthermore, in Figures 8D to 8A, one ceramic substrate was used. However, a plurality of substrates containing various kinds of ceramic materials may be laminated simultaneously.--

B7 Cont.

Please replace the paragraph beginning at page 25, line 1 with the following new paragraph:

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-- In order to evaluate the physical properties of the sheet material produced by the above-mentioned process, a thermal pressing was carried out and the cured product of the sheet was produced. Then, a modulus of elasticity and glass transition temperature of the cured product were measured. The thermal pressing was carried out under the conditions: the produced sheet was sandwiched between the release films and was subjected to a thermal pressing at 200°C and a pressure of 4.9 MPa for 2 hours. The modulus of elasticity and glass transition temperature (Tg) of the cured product at room temperature are shown in the above-mentioned Tables 1 and 2, and the temperature characteristics of the modulus of elasticity are shown in Figure 9, respectively. As shown in Tables 1 and 2, the modulus of elasticity of the cured product at room temperature ranges between about 0.7 GPa and about 8 GPa. As a comparative example, the cured product using an epoxy resin having a modulus of elasticity of 36.5 GPa was prepared. Furthermore, as in the case 2, a cured product in which an epoxy resin having a different glass transition temperature was added also was evaluated. The glass transition temperature was calculated from Tan δ representing the viscosity behavior of the modulus of elasticity based on the temperature characteristics of the modulus of elasticity E' as shown in Figure 10. Figure 10 shows the temperature characteristics of the modulus of elasticity E' of the case 2. From an inflection point of Tan δ, it is confirmed that the glass transition temperature of this mixture is 50°C and 130°C, respectively.--

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